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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	Y. Kubota et al.	EXAMINER: H. Tran	
U.S. SERIAL NO.:	09/506,033	GROUP:	2674
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FOR: LATCH CIRCUIT, SHIFT REGISTER CIRCUIT, LOGICAL CIRCUIT AND IMAGE DISPLAY DEVICE OPERATED WITH A LOW CONSUMPTION OF POWER

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RESPONSE TO OFFICE ACTION

Sir:

The following is in response to the Office Action mailed July 14, 2003, in the above-referenced application. Applicants appreciate the notification of allowable subject matter, i.e., that claims 38-52 are merely objected to, but would be allowable if rewritten in independent form.

With reference to claim 1, Applicants' claimed invention is directed to a latch circuit, including: a first input of a pulse signal, a second input of a clock signal, and an output comprising the pulse signal in synchronization with the clock signal such that the clock signal is smaller in amplitude than the pulse signal. Claim 18 is directed to a shift register circuit made up of a plurality of latch circuits, each latch circuit having a clock signal input control section, which inputs and stops a clock signal, where the clock signal has an amplitude smaller than a pulse signal.

The Applicants' invention is exemplified by the latch circuit diagram of FIG. 3. As shown in FIG. 3, latch circuit LAT includes clock signal input control sections 12 and 13 for inputting a clock signal ck (/ck) and a pulse signal in (/in), where the clock signal has an amplitude smaller than an amplitude of the pulse signal. For example, in the embodiment of FIGS. 1-4, the clock signal is 5 V and the pulse signal is 16 V.

The above-described latch circuit can yield significant benefits. By inputting clock signals having a voltage lower than the pulse voltage of the circuit, the consumption of power by the clock signals is reduced. Moreover, in a shift register circuit constructed by serially connecting a plurality of latch circuits, power consumption is reduced in the shift register circuit and, therefore, the liquid crystal device can operate at a reduced level of power.

With reference to claim 37, Applicants' claimed invention is directed to a CMOS logical circuit, including: a first input signal having a first amplitude and a second input signal having a second amplitude, wherein the amplitude of at least one of the input signals is smaller than a drive voltage of the CMOS logical circuit.

The Applicants' invention as recited in claim 37 is exemplified by FIG. 51, which depicts "first" input signals IN1 and /IN1 having an amplitude of 5 V, and "second" input signals IN2 and /IN2 having an amplitude of 15V. In FIG. 51, the amplitude of input signals IN1 and /IN1 is smaller than the drive voltage Vcc (15 V).

Claims 1-3, 18-21, 37, 53, and 58-64 were rejected under 35 USC 102(e) as being anticipated by U.S. Patent 6,166,725 to Isami et al. (hereinafter "Isami"). This rejection is respectfully traversed.

With reference to FIG. 13 of Isami, as cited in the Office Action, FIG. 13 illustrates a conventional active matrix type liquid crystal display module and driving method (see column 1, lines 59-62). A display data latch clock (D2) "which serves as a display control signal for latching display data" is outputted through a signal line 531 to a data latch circuit of a drain driver 530 (see column 3, lines 5-8). However, Isami

fails to teach or suggest providing a clock signal having an amplitude **smaller** than an amplitude of a pulse signal.

In Isami, data as a first input and the display data latch clock (D2) as a second input are inputted to the drain driver 530 (see FIG. 13), where the display data are processed and outputted from an output circuit 557 of the drain driver 530, as shown in FIG. 19 (see column 6, lines 8-10). However, latch circuit 565 of the drain driver 530 is separate from a level shifter (LS) 556 (see FIG. 20), and therefore it is apparent that the latch circuit 565 has no level shift function. Consequently, the amplitude of the output signal of the latch circuit 565 is the same as that of the input signal, i.e., the display data latch clock (D2).

In the Office Action, bus line 533 in Isami was indicated as corresponding to Applicants' claimed "first input," and signal line 532 was indicated as corresponding to a "second input" (It is assumed that the Examiner meant signal line "531" since reference numeral 532 corresponds to an output). As explained above, the display data latch clock (D2) inputted over signal line 531 has the same amplitude as the output signal of the latch circuit 565 in Isami.

In the Office Action, it was further stated that the fixed common-electrode voltage method, in which voltages applied to the pixel electrodes are twice the voltages applied using the common-electrode voltage inversion method, corresponds to "the clock signal or the pulse signal having amplitude smaller than the amplitude of the pulse signal outputted from the latch circuit" (Office Action, Page 3, first paragraph).

However, it is well known to one of ordinary skill in the art that the fixed common-electrode voltage method and the common-electrode voltage inversion method are merely common methods for driving a liquid crystal device, and do not relate to relative voltage levels of the clock signal or pulse signal in a latch circuit. This is apparent from the disclosure of Isami at column 5, lines 11-18, where it is discussed that the common-electrode voltage method has a disadvantage that an amplitude of a voltage applied to a pixel electrode is twice that of the common-electrode voltage inversion method, "but has advantages that a dot-inversion drive method ... provides

power consumption saving and an excellent display quality," where the active matrix liquid crystal display module depicted in FIG. 13 employs the dot-inversion method (see column 5, lines 11-20).

In other words, the active matrix type liquid crystal display module of FIG. 13 employs only the common-electrode voltage method and does not employ both the common-electrode voltage method and the common-electrode voltage inversion method. As known to one of ordinary skill in the art, the common-electrode voltage method and the common-electrode voltage inversion method are mutually exclusive methods for driving a liquid crystal display device – only one of these drive methods can be used at a time. Therefore, it is impossible to somehow combine a clock signal driven by the common-electrode voltage inversion method with an output signal driven by the common-electrode voltage method.

For at least the reasons discussed above, Isami does not teach or suggest that the clock signal has an amplitude **smaller** than the pulse signal in a latch circuit.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,

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